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TRANSMITTAL OF APPEAL BRIEF (Large Entity)	Docket No. IIZ.008D

In Application Of: **Jun Kanamori**

Serial No.	Filing Date	Examiner	Group Art Unit
09/398,189	September 17, 1999	S. Rao	2814

Invention: **METHOD OF FABRICATING A SEMICONDUCTOR DEVICE WITH SELF-ALIGNED SILICIDE AREAS FORMED USING A SUPPLEMENTAL SILICON OVERLAY**

TO THE COMMISSIONER FOR PATENTS:

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	:	Before the Board of Appeals
Jun Kanamori	:	Appeal No.:
Serial No.: 09/398,189	:	Group No.: 2814
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TABLE OF CONTENTS

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APPEAL BRIEF

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Date: April 29, 2004

Sir:

This is an appeal from the final rejection of claims 2-6, 24-34, 36 and 38, which claims were finally rejected in the Office Action dated September 29, 2003. A Notice of Appeal was filed on March 1, 2004.

I. REAL PARTY IN INTEREST

This application is assigned to Oki Electric Industry Co., Ltd., which is the real party in interest.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences that will directly affect or be affected by or have a bearing on the Board's decision in this pending appeal.

III. STATUS OF THE CLAIMS

Claims 2-6, 24-34, 36 and 38 are present in this application, and the rejection thereof is hereby appealed.

IV. STATUS OF AMENDMENTS

Subsequent to the Final Office Action dated September 29, 2003, Applicant submitted an Amendment under 37 C.F.R. 1.116 on December 29, 2003. Independent claims 24 and 30 were respectively amended to include the features of dependent claims 35 and 37. Claims 35 and 37 were canceled. Dependent claims 36 and 38 were amended merely to improve antecedent.

In the Advisory Action dated February 12, 2004, the Examiner indicated that the Amendment under 37 C.F.R. 1.116 on December 29, 2003, would be entered for purposes of appeal. The Examiner also suggested amendments to improve dependent claims 36 and 38.

In the Amendment under 37 C.F.R. 1.116 dated March 1, 2004, dependent claims 36 and 38 were amended as suggested by the Examiner in the Advisory Action

dated February 12, 2004. The copy of claims in Appendix A incorporates the above noted amendments therein.

V. SUMMARY OF THE INVENTION

The present invention relates to a method of fabricating a semiconductor device using a self-aligned silicide (salicide) process.

As shown in Fig. 2A, a buried oxide (BOX) layer 114 having a thickness of 100 nm to 200 nm is formed on silicon substrate 112. A field oxide layer 116, and a silicon on insulator (SOI) layer 118 of fully depletion type (FD) having a thickness of 50nm to 100 nm, are formed on BOX layer 114 (page 8, lines 11-16). Subsequently, a gate oxide layer 120 and a poly-silicon gate layer 122 are formed in order on SOI layer 118. A gate side wall layer 124 is then formed on SOI layer 118 to surround poly-silicon gate layer 122 and gate oxide layer 120 (page 8, lines 16-22).

As shown in Fig. 2B, the upper surface of the structure as described with respect to Fig. 2A is then covered with cobalt layer 126 and titanium nitride layer 128 in order, by sputtering (page 8, line 23 through to page 9, line 4).

A first rapid thermal anneal (RTA) process is then carried out at about 500°C to 600°C, so that silicide reactions occur between SOI layer 118 and cobalt layer 126, and between poly-silicon gate layer 122 and cobalt layer 126, to thus form high resistance cobalt silicide regions 130 in SOI layer 118 and high resistance cobalt silicide region 132 in poly-silicon gate layer 122, as shown in Fig. 2C. Portions of cobalt layer 126 and

titanium nitride layer 128 remaining after the first rapid thermal anneal process are then removed, to complete the structure as shown in Fig. 2C (page 9, lines 5-16).

As shown in Fig. 2D, a poly-silicon layer 136 having a thickness of 5 nm to 10 nm is formed as a supplemental silicon layer on the entire surface of the structure shown in Fig. 2C (page 9, lines 17-21).

Then, a second rapid thermal anneal (RTA) process is carried out at a temperature of 750°C to 850°C on the structure shown in Fig. 2D. During the second rapid thermal anneal process, silicon contained in SOI layer 118 and in poly-silicon layer 136 react with high resistance cobalt silicide region 130 to form low resistance cobalt silicide regions 138, and silicon contained in poly-silicon gate layer 122 and in poly-silicon layer 136 react with high resistance cobalt silicide region 132 to form low-resistance cobalt silicide region 140, as shown in Fig. 2E (page 9, line 22 through to page 10, line 10). Portions of poly-silicon layer 136 remaining after the second thermal anneal process are then removed, to complete the structure shown in Fig. 2E.

Since silicon is provided from poly-silicon layer 136 (supplemental silicon layer), and not only from SOI layer 118 and poly-silicon gate layer 122 during the second rapid thermal anneal, there is enough silicon provided so that silicon remains in SOI layer 118 after the second rapid thermal anneal is completed. Therefore, low-resistance wiring can be realized by a salicide process on an SOI layer 118 initially formed as thin as less than 70 nm (page 10, lines 16-22).

In an embodiment described beginning on page 17, line 2 of the application with

respect to Figs. 5A-5D, different type impurities are doped into the supplemental silicon layer above the N-channel region and the P-channel region of a CMOS device.

Before the second rapid thermal anneal process, poly-silicon layer 436 is formed over the entire structure as a supplemental silicon layer, as shown in Fig. 5A (page 18, lines 19-21).

Then, the P-channel region is covered with photo-resist layer 450 and an n-type impurity is doped into poly-silicon layer 436 at the N-channel region by ion implantation, so that the supplemental silicon layer becomes an n-doped silicon layer 436N as illustrated in Fig. 5B (page 18, line 22 through to page 19, line 2). Thereafter, the N-channel region is covered with photo-resist layer 452 as shown in Fig. 5C, and a p-type impurity is doped into poly-silicon layer 436 at the P-channel region by ion implantation, so that the supplemental silicon layer becomes a p-doped silicon layer 436P (page 19, lines 5-8). According to this embodiment, impurities are doped into the supplemental silicon layer 436, so that the remaining silicon after the second rapid thermal anneal process can be removed at a high etching rate with high selectivity (page 19, lines 21-24).

VI. ISSUES

Claims 2-6, 24-34, 36 and 38 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPR), the Doan et al. reference (U.S. Patent No. 5,946,595), the Besser et al. reference (U.S. Patent No.

6,165,903), and the Xiang et al. reference (U.S. Patent No. 6,015,752).

Accordingly, one issue presented is whether or not the methods of claims 2-6, 24-34, 36 and 38 are obvious in view of the combined teachings of Applicant's admitted prior art, the Doan et al. reference, the Besser et al. reference, and the Xiang et al. reference.

VII. GROUPING OF CLAIMS

Appellant respectfully wishes to group all of claims 2-6, 24-34, 36 and 38 together.

VIII. ARGUMENTS

A feature of the preferred embodiments of the present application is that a silicide layer is formed in a first rapid thermal anneal (RTA) process, the silicide layer is masked with a supplemental silicon layer, and then a second RTA process is carried out whereby the supplemental silicon layer provides the silicon contained in the silicide layer of the processed structure. The embodiments of the present application as claimed are used in connection with a thin SOI substrate, in which a silicon layer is formed on a BOX insulation layer.

That is, claim 24 includes in combination "providing a semiconductor substrate which has a silicon region located on an insulating layer formed in the semiconductor substrate", wherein "a thickness of the silicon region is in a range of 50-100 nm". Claim

30 includes in combination "providing a field oxide layer and a silicon on insulator layer on the buried oxide layer", wherein "a thickness of the silicon on insulator layer is in a range of 50-100 nm".

In view of the use of the supplemental silicon layer, generation of voids in the substrate can be reduced. The embodiments of the present application are therefore especially useful in connection with an SOI substrate having a thin silicon layer, within the range of 50-100 nm, as specifically featured in independent claims 24 and 30.

Appellant respectfully notes that of the prior art as relied upon in the above noted rejection, only Applicant's admitted prior art as described with respect to Figs. 1A-1C is directed to an SOI structure. That is, of the prior art taken as a whole, only Applicant's admitted prior art is directed to an SOI structure in which the device is formed on a thin SOI layer having a thickness of 50 nm to 100 nm. However, a supplemental silicon layer is not used in connection with Applicant's admitted prior art. Thus, a device including a thin SOI layer with irregular thickness manufactured as in Applicant's admitted prior art, will include thinner parts of the SOI layer that may be salicided entirely to create voids.

Appellant respectfully emphasizes that the various secondary references as relied upon by the Examiner do not teach SOI structures. In other words, the secondary references are not directed to devices built on SOI layers having thickness in the range of 50-100 nm, and thus do not recognize and are not concerned with the problem of thinner parts of an SOI layer being salicided entirely to create voids. That is,

none of the prior art as relied upon recognizes the use of a supplemental silicon layer to overcome the problem of thinner parts of an SOI layer being salicided entirely to create voids. This should be clear because the secondary references do not include thin SOI layers.

Particularly, the Besser et al. reference is directed to ultra-shallow junction formation by reducing the amount of silicon consumption during salicidation, so that **source/drain junctions** may be made shallower and to avoid junction leakage (column 4, lines 34-36). The preferred embodiments of the Besser et al. reference provide sufficient distance between the bottom of the silicide and the bottom of the source/drain junction so that there will be no junction leakage (column 3, lines 10-13). The structures as illustrated in Figs. 7-10 of the Besser et al. reference are formed on silicon substrate 30. Silicon substrate 30 is not described as an SOI layer in a range of 50-100 nm. The Besser et al. reference thus does not recognize and is not concerned with the problem of thinner parts of an SOI layer being salicided entirely to create voids. One of ordinary skill thus would not be motivated to modify Applicant's admitted prior art in view of the Besser et al. reference to arrive at the method of claims 24 and 30, because the Besser et al. reference does not include an SOI layer and is not concerned with preventing thinner parts of an SOI layer from being salicided entirely to create voids. The Besser et al. reference is concerned with ultra-shallow junction formation and avoiding junction leakage.

The Doan et al. reference is relied upon to show doping of what has been

characterized as a supplemental silicon layer of the claims, so that the supplemental silicon layer can be etched at a faster rate. However, the Doan et al. reference as relied upon also is not directed to an SOI structure in which a device is formed on a thin SOI layer having a thickness of 50 nm to 100 nm. The Doan et al. reference does not recognize and is not concerned with the problem of thinner parts of an SOI layer being salicided entirely to create voids.

Moreover, column 6, lines 7-17 of the Doan et al. reference as relied upon in the prior art rejection, describes polysilicon layer 24 deposited on **thin titanium layer 22**, as illustrated in Fig. 3. Implant mask 32 is formed on polysilicon layer 24 as shown in Fig. 8, and ions are then implanted into polysilicon layer 24 through implant mask 32, as described in column 6, lines 18-21. After removal of mask 32, the non-implanted portions of polysilicon layer 24 are etched and removed, as described in column 6, lines 31-34. A rapid thermal anneal is then conducted as described in column 6, lines 62-65, to form titanium silicide region 34 as illustrated in Figs. 10 and 11. A final heat treatment is then preferably conducted to convert the Ti_3Si_5 regions to a species substantially composed of $TiSi_2$, **to conclude the local interconnection formation method** (column 7, lines 34-39).

Accordingly, polysilicon layer 24 as described in column 6, lines 7-17 of the Doan et al. reference as relied upon in the prior art rejection, is not a supplemental silicon layer as featured in claim 24 of the present application. That is, polysilicon layer 24 of the Doan et al. reference is not formed on a first-reacted silicide region as featured in

claim 24, but is in contrast formed on titanium layer 22 as described with respect to Fig. 3. Polysilicon layer 24 of the Doan et al. reference does not react with a first-reacted silicide region during a second rapid thermal annealing, to convert a first-reacted silicide region into a second-reacted silicide region, as featured in claim 24. Polysilicon layer 24 of the Doan et al. reference is merely transformed into a local interconnection, and does not function as a supplemental silicon source for a silicide region during a rapid thermal annealing process. Appellant therefore respectfully submits that since the Doan et al. reference does not include a supplemental silicon layer as featured in claims 24 and 30, the Doan et al. reference does not overcome the deficiencies of the previously combined prior art.

The Xiang et al. reference has been relied upon to show a CMOS device including both n-channel and p-channel transistors. However, the Xiang et al. reference is merely directed to CMOS devices with ultra-shallow junctions. As described in column 4, lines 15-20 of the Xiang et al. reference with respect to Fig. 1, a conventional transistor structure is formed in a conventional manner on substrate 10 as including source/drain regions comprising a shallow extension region 11A and a heavily doped (HD) region 11B. The Xiang et al. reference is not directed to an SOI structure in which a device is formed on a thin SOI layer having a thickness of 50 nm to 100 nm. The Xiang et al. reference does not recognize and is not concerned with the problem of thinner parts of an SOI layer being salicided entirely to create voids. One or ordinary skill thus would not be motivated to modify Applicant's admitted prior art in view of the

Xiang et al. reference to arrive at the method of claims 24 and 30, because the Xiang et al. reference does not include an SOI layer and is not concerned with preventing thinner parts of an SOI layer from being salicided entirely to create voids.

Accordingly, since the secondary references as relied upon do not include thin SOI layers, the secondary references would provide no motivation to modify Applicant's admitted prior art as suggested to prevent thinner parts of an SOI layer from being salicided entirely to create voids. Appellant therefore respectfully submits that claims 2-6, 24-34, 36 and 38 would not have been obvious in view of the prior art as relied upon, and that this rejection is improper for at least the above reasons, and should thus be reversed.

Consequently, favorable reconsideration and allowance of all claims by the Honorable Board of Patent Appeals and Interferences is respectfully requested.

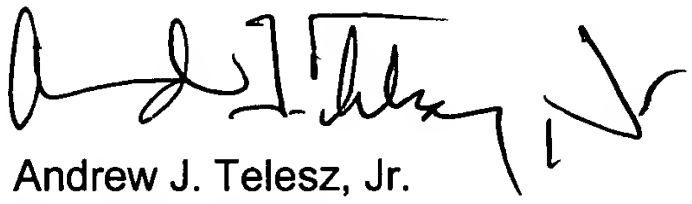
In the event that there are any outstanding matters remaining, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

The required fee of $330.00 under 37 C.F.R. 1.17(c) for filing this Appeal Brief is attached hereto.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS, P.L.L.C.



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Enclosures: Appendix A –Claims

Appendix A- Claims

Claim 2: The method according to claim 30, wherein the material to be silicided comprises cobalt.

Claim 3: The method according to claim 30, wherein the material to be silicided comprises titanium.

Claim 4: The method according to claim 30, wherein the supplemental silicon layer is poly-silicon formed by a chemical vapor deposition technique.

Claim 5: The method according to claim 30, wherein the supplemental silicon layer is amorphous silicon formed by a sputtering technique.

Claim 6: The method according to claim 30, further comprising:

selectively removing non-reacted silicon from the second-reacted silicide region after the second rapid thermal annealing.

Claim 24: A method for fabricating a semiconductor device, comprising:

providing a semiconductor substrate which has a silicon region located on an insulating layer formed in the semiconductor substrate;

forming a metal layer on the silicon region of the semiconductor substrate;

performing a first rapid thermal annealing on the semiconductor substrate to

form first-reacted silicide regions;

forming a supplemental silicon layer on the first-reacted silicide regions;

doping an impurity into the supplemental silicon layer; and

performing a second rapid thermal annealing to convert the first-reacted silicide regions into second-reacted silicide regions, by reaction of the supplemental silicon layer with the first-reacted silicide regions,

the semiconductor device including a p-channel MOS transistor having p-type source and drain diffusion layers, and including an n-channel MOS transistor having n-type source and drain diffusion layers,

said doping comprising doping the impurity into the supplemental silicon layer so that only the supplemental silicon layer formed over the p-channel MOS transistor is doped, or so that only the supplemental silicon layer formed over the n-channel MOS transistor is doped, and

a thickness of the silicon region is in a range of 50-100 nm.

Claim 25: The method according to claim 24, wherein the metal layer comprises cobalt.

Claim 26: The method according to claim 24, wherein the metal layer comprises titanium.

Claim 27: The method according to claim 24, wherein the supplemental silicon layer is poly-silicon formed by a chemical vapor deposition technique.

Claim 28: The method according to claim 24, wherein the supplemental silicon layer is amorphous silicon formed by a sputtering technique.

Claim 29: The method according to claim 24, further comprising:

selectively removing non-reacted silicon from the second-reacted silicide regions after the second rapid thermal annealing.

Claim 30: A method for fabricating a semiconductor device comprising:

providing a silicon substrate;

providing a buried oxide layer on the silicon substrate;

providing a field oxide layer and a silicon on insulator layer on the buried oxide layer;

providing a gate oxide layer on the silicon on insulator layer;

providing a poly-silicon gate layer on the gate oxide layer;

providing a gate side wall layer on the silicon on insulator layer to surround the poly-silicon gate layer and the gate oxide layer;

providing a material to be silicided on a surface of the semiconductor device including the poly-silicon gate layer, the gate side wall layer, the silicon on insulator layer and the field oxide layer;

performing a first rapid thermal annealing process to form first-reacted silicide regions in the poly-silicon gate layer and in source/drain active areas of the silicon on insulator layer;

removing non-reacted material from the first-reacted silicide regions;

providing a supplemental silicon layer over the surface of the semiconductor device after the non-reacted material is removed;

doping the supplemental silicon layer; and

performing a second rapid thermal annealing process to convert the first-reacted silicide regions into second-reacted silicide regions, by reaction of the supplemental silicon layer with the first-reacted silicide regions,

the supplemental silicon layer preventing the poly-silicon gate layer and the silicon on insulator layer from being completely silicided,

the semiconductor device including a p-channel MOS transistor having p-type source and drain regions, and including an n-channel MOS transistor having n-type source and drain regions,

said doping comprising doping an impurity into the supplemental silicon layer so that only the supplemental silicon layer provided over the p-channel MOS transistor is doped, or so that only the supplemental silicon layer provided over the n-channel MOS transistor is doped, and

a thickness of the silicon on insulator layer is in a range of 50-100 nm.

Claim 31: The method according to claim 24, wherein said doping comprises doping a p-type impurity into the supplemental silicon layer so that only the supplemental silicon layer over the p-channel MOS transistor is doped p-type.

Claim 32: The method according to claim 24, wherein said doping comprises doping an n-type impurity into the supplemental silicon layer so that only the supplemental silicon layer over the n-channel MOS transistor is doped n-type.

Claim 33: The method according to claim 30, wherein said doping comprises doping a p-type impurity into the supplemental silicon layer so that only the supplemental silicon layer over the p-channel MOS transistor is doped p-type.

Claim 34: The method according to claim 30, wherein said doping comprises doping an n-type impurity into the supplemental silicon layer so that only the supplemental silicon layer over the n-channel MOS transistor is doped n-type.

Claim 36: The method according to claim 24, wherein the thickness of the silicon region is in a range of 50-70 nm.

Claim 38: The method according to claim 30, wherein the thickness of the silicon on insulator layer is in a range of 50-70 nm.